AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0037] with the following amended paragraph:

[0037] Figure 3 shows a block diagram of a PAM transmit modulation using a polar alternative in the form of direct amplitude and phase modulation. The real and imaginary filter outputs Re{s(t)} and Im{s(t)} are input to a polar coordinate converter 18. The polar coordinate converter 18 outputs angle and magnitude values ang{s(t)} and mag{s(t)}, respectively. The direct phase modulation might be performed by modulating the oscillator 20 tuning input in a feed-forward manner with a possible PLL loop compensation method. The direct amplitude modulation might be performed by a voltage, current or digitally controlled power amplifier 22 or by regulating the supply voltage to a constant-envelope power amplifier. A preferred embodiment uses a digital pulse slimming circuit. This method is likely to be the best choice for digital integration of mobile RF transceivers because it does not use the RF/analog-intensive up-conversion modulator.

Please replace paragraph [0044] with the following amended paragraph:

[0044] Generating the output of the transmit filter shown in Figures 4a[[-b]] and 4b requires the generation of two clock signals, the baseband symbol clock and the baseband chip clock. Generation of the clock signals can be very costly in terms of area and power if the baseband chip clock is not an integer multiple or division of an available clock. Further, the reference clock, FREF, must be a multiple of 1 MHz. This can be significant, since many communication systems do not use a reference clock that is an integer multiple 1 MHz and, therefore, an additional clock must be generated. For

example, CDMA uses a 19.2 MHz reference clock and PDC (Personal Digital Cellular) uses a 12.6 MHz reference clock.

Please replace paragraph [0052] with the following amended paragraph:

[0052] Figure 7b illustrates a schematic view of a portion of the search circuit 102 that determines the length of a pulse on DT_TX to ensure that it is a valid "1" data state. Logic 118 counts CKR clock cycles between a detected rising transition and a detected falling transition. This count is shown as Q_CNT. After the falling transition, OSR_ROUND, the expected length of a valid "1" pulse, is compared to Q_CNT in logic 120. If OSR_ROUND and Q_CNT are within a predetermined threshold (for example, two CKR clock cycles), DT_FOUND is enabled at an output of register/latch 122; otherwise DT_MISS is enabled at an output of register/latch 124.

Please replace paragraph [0056] with the following amended paragraph:

[0056] Figures 10a[[-c]] through 10c illustrate curves for various state transitions based on the previous two symbol values, DT_0[-2] and DT_0[-1]. In Figure 10a, starting from a state of "00", if the current DT_0 is a "1", the next state will be "01". On the other hand, if the current DT_0 is a "0", the next state will be "00". In Bluetooth, the output will vary between "+1" and "-1". A state of "00" will be at -1. If the current DT_0 is a "0", the output will remain at "–1" and the new state will be "00". If the current DT_0 is a "1", the output will transition to "0" and the new state will be "01". From state "01" if the current DT_0 is "0", the output will transition from a start value of "0" to an end value of "0", but because of the preceding "01" transition, the output will have an upwards curve between the starting and ending points. The new state will be "10". If the

current DT_0 is "1" from state "01", the output will transition from a start value of "0" to an end value of "+1". The new state will be "11".

Please replace paragraph [0073] with the following amended paragraph:

[0073] Figure 15 illustrates a block diagram of a circuit 101 that could be used in order to reduce the number of sample points generated, either in a deterministic or random manner. Figure 15 is similar to Figure 6, with the addition of pass-thru and latch logic circuit 170 interposed before the filter circuit 108. Pass-thru and latch logic 170 receives DT_STATE from the state circuit 104 and DT_PH_I and DT_PH_I from phase tracking circuit 106. These signals are passed through to filter circuit 108 responsive to control signals from other logic (not shown) that determines whether a sample point 90 should be generated.